ZnO Nanowires Synthesized by Vapor Trapping CVD Method

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A chemical vapor deposition (CVD) process modified with vapor trapping method has been used to synthesize *n*-type ZnO nanowires with high carrier concentration without incorporating impurity dopants. With this method, a spatial variation of synthesis condition was created and the donors were directly introduced into the nanowires during the synthesis process. Electron microscopy and electrical transport studies show that nanowires having distinct morphologies and electrical properties were obtained at different locations in the CVD system. The vapor trapping method elucidates the effect of synthesis conditions, and provides an approach to control nanowire growth for tailorable device applications.

Introduction

In recent years, much effort has been invested to study quasi-one-dimensional materials because of their unique quantum properties, and their potential to be integrated into nanoscale electronic and optoelectronic devices. Nanowires of various compound semiconductors, such as GaN,[1,2] In_2O_3,[3,4] Si_3N_4, Ga_2O_3,[5] and MgO[6] have been synthesized successfully. Another new system attracting increasing attention is zinc oxide (ZnO), which is a *II*−*VI* compound semiconductor with a wide and direct band gap of 3.37 eV at room temperature. ZnO is known to have wurtzite structure with lattice constant $a = 3.249$ Å, $c = 5.207$ Å. Its large exciton binding energy (60 meV), which is much greater than the thermal energy at room temperature, makes it a promising candidate for applications in blue-UV light emission and room-temperature UV lasing.[7] Furthermore, its high piezoelectric constant ($d_{33} = 246$) makes it a highly valuable material for fabricating mechanical devices, such as acoustic transducers, sensors, and actuators.[8] ZnO nanowires synthesis has been reported using many different approaches, for example sputter deposition,[9] template-assisted growth,[10] and chemical vapor deposition (CVD).[11] To improve the performance of actual electronic devices, nanowires with better electrical properties should be prepared in advance. In our experiment, we have modified the CVD synthesis process with a vapor trapping design to facilitate and control the charge carrier concentration. The as-grown nanowires exhibit *n*-type semiconducting behavior with high carrier concentration.[12]

Nanowire Synthesis

Nanowires were synthesized via a vapor−liquid−solid (VLS) growth mechanism.[13] The VLS process took place in a horizontal quartz tube placed in a rapid thermal furnace. It had been suggested that native defects, such as zinc interstitials and oxygen vacancies, contribute to the *n*-type semiconducting behavior of ZnO, and these defects serve as donors with a binding energy of 30−60 meV.[14,15] For the purpose of introducing more native defects, a quartz vial placed in the quartz tube was used to create a zinc-rich environment in the system. Because synthesis was conducted at 1 atm, the rate of zinc vapor diffusing from the vial was relatively low; therefore, a high concentration of zinc vapor was maintained inside the vial creating a high zinc concentration condition with dilute oxygen content. As a result, it yields a zinc vapor concentration decrease from inside to outside of the vial. This unique feature consequently facilitates various reaction conditions and produces a large amount of residual native defects in the ZnO nanowires.

Clean silicon (Si 001) chips were prepared as substrates in the CVD system. Figure 1 shows a schematic

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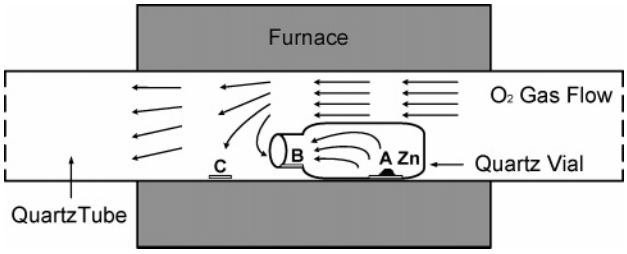

Figure 1. Schematic illustration of the CVD system with a horizontal quartz tube placed in a furnace. A small quartz vial inside the quartz tube is used to trap zinc vapor during the synthesis process.

illustration of the CVD furnace including a horizontal quartz tube of 1-in. diameter. In the quartz tube, Chip A was placed close to the bottom of a quartz vial, Chip B was placed at the bunghole, and Chip C was placed 2.5 cm away from the small quartz vial. Pure zinc powder (99.9% Alfa Aesar) spread on Chip A served as the raw source material. Colloidal gold (Au) nanoparticles with diameter of 30 nm deposited on both Chip B and Chip C served as catalysts in this VLS synthesis mechanism. Once the temperature went above the melting point of zinc metal (420 °C), zinc would gradually vaporize to fill the quartz vial and then diffuse to Chip B and then to Chip C. The Au nanoparticles on the silicon chips (B and C), which had formed liquid droplets, became super-saturated with zinc vapor. The nucleation of zinc oxide then began with the arrival of oxygen gas (O_2). According to the crystal growth theory, when the droplets reached a critical radius, ZnO began to precipitate. The growth continued along one favorable direction in which the surface free energy was minimized. Synthesis was carried out in the following steps. First, the quartz tube was evacuated to 10^{-2} Torr, then it was purged with Argon (Ar) gas to maintain a 1 atm inert ambient. Second, the furnace temperature was rapidly elevated to 700 °C in 10 min with a constant Ar gas flow of 90 sccm. Third, the set-point temperature (700 °C) was maintained for twenty minutes. Fourth, oxygen gas (2% concentration mixed with 98% Ar) was then flown through the quartz tube for 30 min. At the end of the process, both Chip B and Chip C appear white on the substrate surfaces.

Characterizations

In this vapor trapping CVD synthesis, we arranged the two growth chips, B and C, at different positions inside the system, in order to understand the effect on growth by the variation in the zinc and oxygen concentration distribution. After synthesis, material characterizations, including electron microscopy and electrical transport measurements, were performed. The objective was to verify and distinguish the morphology change and carrier concentration difference between the nanowires grown on Chip B and Chip C.

A. Electron Microscopy. A field emission scanning electron microscopy (FE-SEM, FEI/Philips XL-30) image (Figure 2) shows that nanowires grown on Chip C have diameters ranging from 20 to 200 nm with average length about 30 μm. These nanowires presented on Chip C can be regarded as having been synthesized using a more traditional VLS method that many researchers have reported. We found nanowires were distributed

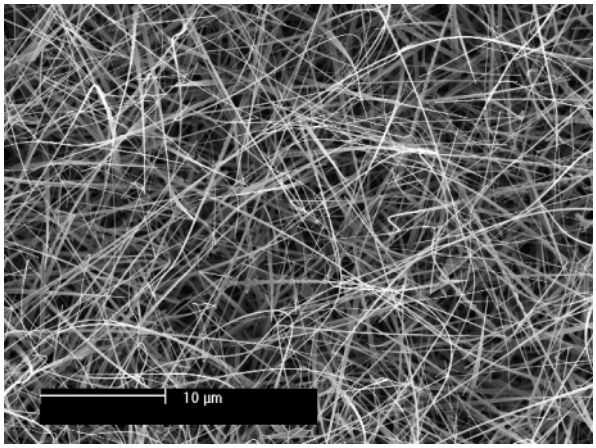

Figure 2. SEM image shows high density of ZnO nanowires grown randomly on Chip C placed outside the quartz vial.

uniformly all over Chip C. In comparison, ZnO crystals were found to grow in various geometrical shapes on Chip B. Though the microstructure differences of ZnO have been well-characterized,[16] the variety obtained within such a small area on the silicon substrate with one experimental run has not been previously reported. To illustrate those differences, a series of SEM pictures (Figure 3) with same magnification (scale bar 10 μm) has been taken from the inner edge to the outer edge of Chip B, sequentially at locations b_1, b_2, b_3, b_4, b_5, and b_6 as indicated schematically in Figure 3a. Only locations b_1 and b_2 are from the region on the substrate where Au catalysts deposition did not reach, and therefore it was found that vapor−solid (VS) process occurred during the synthesis. As shown in Figure $3b_1$, a sheet of ZnO tabular crystal was formed. The inset is a zoom-in view showing the hexagonal structure crystal just nucleated and ready to grow. Figure $3b_2$ shows prismatic hexagonal rods of ZnO grown at b_2 area. In the region where Au catalysts were deposited, well-grown ZnO nanowires were observed at b_3 area (Figure $3b_3$). Those nanowires having diameters around 20−300 nm were very similar in geometry to the nanowires retrieved from Chip C and could be used to make nanowire devices. Moreover, moving outward to the bunghole, at region b_4 we found that crystals, instead of growing longer, started to grow on the surface of the nanowires because of the polarization induced growth[17] (Figure $3b_4$). Once it began to grow on the surface of individual nanowires, ZnO dendrite structures were formed, for example, comblike structure was created due to the polar surface growth shown in Figure $3b_5$. Because of the higher oxygen concentration at b_6 area, ZnO crystals grew into thicker needlelike shapes. Figure $3b_6$ is a snapshot of the outer edge where many needlelike dendrite crystals with micrometer diameters could be found.

The variation of crystal growth on Chip B was due to the spatial change of Zn and O_2 vapor pressure inside the quartz vial. The synthesis system could be simplified as a one-dimensional steady-state diffusion model from

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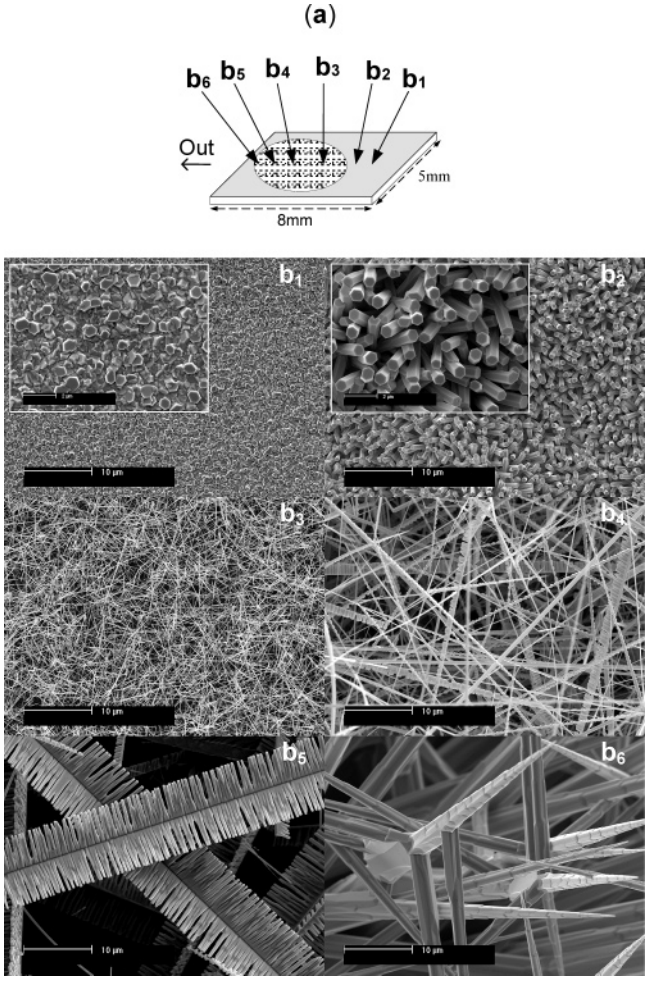

Figure 3. (a) Six areas on Chip B substrate have been analyzed by SEM. Starting from the outer part of Chip B, locations b_1, b_2, b_3, b_4, b_5, and b_6 are labeled. The shaded circle indicates the region of Au catalysts deposition. (b_1) ZnO crystal sheets have just nucleated and started to grow. Inset is a close-up of the substrate surface showing the evidence of growth. (b_2) ZnO rods can be seen at b_2 area on Chip B. Higher magnification inset with scale bar 2 μm shows clear hexagonal crystal structure of ZnO rods. (b_3) Good-quality ZnO nanowires obtained at b_3 area. With high aspect ratio, nanowires have diameters from 20 to 300 nm and average length of ~20 μm. (b_4) On the surface of an individual nanorod, it can be found that ZnO crystals initially grow perpendicular to the surface. (b_5) Crystals start to nucleate and grow from the surface on one single nanowire, forming a comb structure. (b_6) Thick ZnO needle can be found at the outer edge. With sufficient oxygen concentration, wires with larger diameter are grown.

the fundamental mass transfer perspective.[18] In this model, crystal growth rate and nucleation rate are determined by zinc and oxygen vapor concentration ratio. At the inner part of the chip, oxygen had the lowest concentration and zinc had the highest vapor pressure. As a result, Chip B had a surface-reaction-limited situation dominated at inner regions (b_1, b_2) where the mass transfer rate was higher due to the larger Zn/O_2 vapor pressure ratio. On the other hand, at the outer areas (b_5, b_6) a lower pressure difference resulted in a higher nucleation rate that made nanowires grow into branch "buds" instead of growing longer.

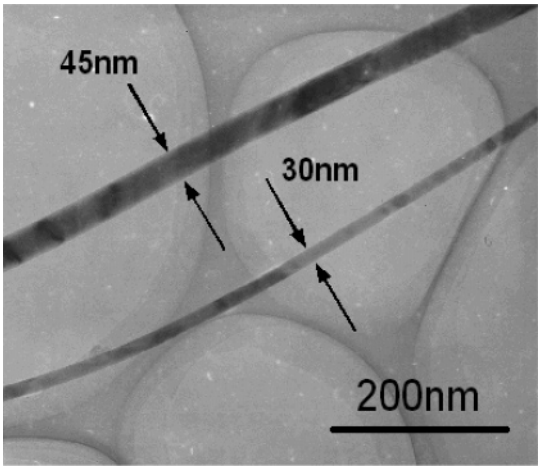

Figure 4. Transmission electron microscopy (TEM) image demonstrates two ZnO nanowires with different diameters of 30 and 45 nm. The scale bar is 200 nm.

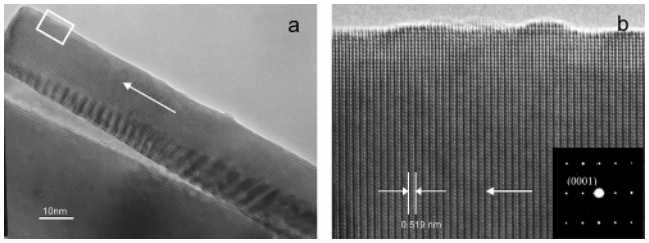

Figure 5. (a) A ZnO nanowire has about 20 nm diameter and is single-crystal grown in one direction. (b) HRTEM image of the rectangular section in Figure 5a shows ZnO crystal lattice fringes with spacing of 0.52 nm. The inset is a selected-area electron diffraction (SAED) pattern confirming the lattice spacing and the *c* axis [0001] is the growing direction.

The effect of mass-transfer-controlled process could thus be clearly demonstrated in the above SEM analysis. Therefore, one learns that zinc and oxygen vapor pressure difference plays an important role during synthesis, and the morphology of crystal is determined by the relative rate of surface reaction with respect to the mass transfer rate. Conclusively, to obtain high-quality nanowire growth such as those obtained at location b_3, it is important to balance a proper mass transfer to surface reaction ratio.

Transmission electron microscopy (TEM, FEI/Philips CM20) observation was done to examine the synthesized ZnO nanowires. A low-magnification TEM image (Figure 4) presents two ZnO nanowires with different diameters (30 and 45 nm) obtained from Chip B. The high-resolution transmission electron microscopy (HRTEM) photos shown in Figure 5 indicate that the as-grown ZnO nanowires have single-crystal structure. Figure 5a illustrates a nanowire grown in only one direction. A high-magnification image shown in Figure 5b (taken from the rectangular box in 5a) shows lattice spacing is close to 0.52 nm. The corresponding selected area electron diffraction (SAED) pattern (insert) suggests that ZnO nanowires were growing along the [0001] lattice plane direction which is the *c* axis.[19–21] Energy-

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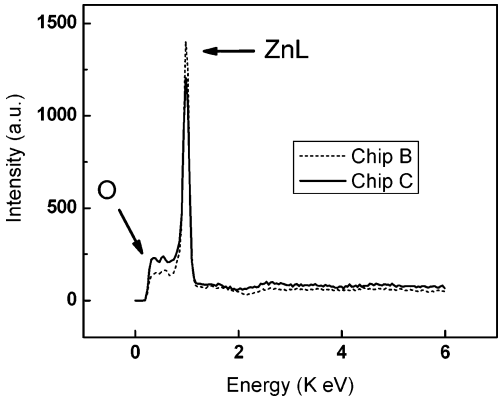

Figure 6. EDS showing that oxygen and zinc spectra collected from Chip B nanowires have lower O peak and higher Zn (L line) peak within energy range 0−6 keV than Chip C nanowires.

dispersive X-ray spectroscopy (EDS) data acquired from two individual nanowires (one from Chip B shown in dashed line, and one from Chip C shown in solid line) shown in Figure 6 demonstrates qualitatively that Chip B nanowires have less oxygen and more zinc in composition as compared with that in Chip C. This result reveals that Chip B nanowires should have more oxygen vacancies and zinc interstitials, which are *n*-type donors.

B. Electrical Properties. To investigate the electrical transport properties, ZnO nanowires were first dispersed in isopropyl alcohol and then deposited onto a p^{++} silicon chip capped with 500 nm of SiO_2. The p^{++} silicon layer acted as the back-gate in the field effect transistor configuration. Photolithography was utilized to place the bi-layer metal contacts on individual ZnO nanowires. Two metals, titanium (Ti) and gold(Au), were carefully selected for the lead materials. Due to the similar work function of Ti (4.33 eV) and ZnO (4.3 eV), an Ohmic contact between the two materials can be formed which is crucial in making efficient devices. After coating with a thin layer of Ti (10 nm), the 500-nm Au layer was then deposited to complete a source−drain−gate three-terminal configuration shown in Figure 7a. Field effect transistors (FETs) were then fabricated using the nanowires selected from Chip B (b_3 region) and Chip C. Figure 7b inset is a SEM image showing a FET made by a single Chip B nanowire indicated by the white arrow.

Electrical transport measurements were conducted by sweeping V_{ds} and V_g. In general, source-drain current versus drain bias voltage ($I_{ds}-V_{ds}$) was measured (Figure 7b) at zero gate voltage ($V_g = 0$) to estimate the conductivity of these two nanowire devices. $I_{ds}-V_{ds}$ curves simply suggest that nanowires on Chip B, having more donors, yield higher electrical conductivity than those on Chip C. Based on the Drude model, assuming the entire source-drain potential was dropped across the nanowires, then we can obtain an estimate giving a lower bound of the nanowire conductivity.[22] The FET fabricated by Chip B nanowire has a radius (r_B) of 60 nm and channel length (L_B) of 7.6μm; the FET fabricated by Chip C has radius (r_C) of 44 nm and length (L_C) of 6.7μm. Their conductivities estimated from those

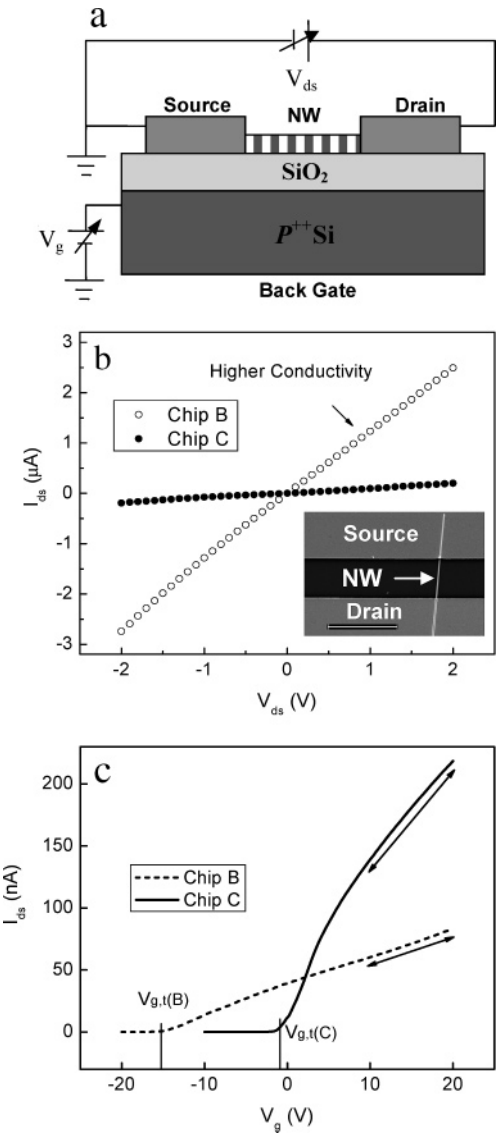

Figure 7. (a) Nanowire FET illustration showing the three-terminal configuration. Ti/Au was used to form metal contacts and Si−SiO_2 substrate served as the backgate. (b) $I_{ds}-V_{ds}$ curves measured from two distinct nanowire FETs show conductivity change due to different doping concentration. Inset is a SEM image of a nanowire FET fabricated by photolithography with scale bar 10 μm. (c) Source-drain current versus gate voltage ($I_{ds}-V_g$) measurement shows that the two FETs have different threshold voltages at −15.5 and −1.3 V, respectively.

parameters are 8.64Ω^{-1}cm^{-1} and 1.02Ω^{-1}cm^{-1}, respectively. In addition, we examined whether the carrier concentration difference was indeed increased and the conductivity improvement was not merely a result of the geometry change. From the threshold voltages given in $I_{ds}-V_g$ curves (Figure 7c), we can compute carrier concentration n using $n = -(V_{g,t}/e)(2\pi\epsilon\epsilon_0 V_{ds}/\ln(2h/r))$.[23] We obtain the carrier concentration of Chip B nanowire approximately 7.46×10^7 cm^{-1}, and that of Chip C is $\sim 5.64 \times 10^6$ cm^{-1} from the measured threshold voltages ($V_{g,t}$) −15.5 V and −1.3 V, showing a difference of one order of magnitude. Furthermore, their mobilities can also be calculated to be 21.7 cm^2/Vs and 80 cm^2/Vs, respectively, by the relation $\mu_e = (dI/dV_g)/(2\pi\epsilon\epsilon_0 V_{ds}/L\ln$-

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$(2h/r))$[23] where $V_{ds} = 0.1$ V, $\epsilon = 3.9$, $h = 500$ nm (gate oxide layer thickness), and the transconductance values $dI/dV_g = 2.2 \times 10^{-9}$A/V for Chip B nanowire, and 8.29×10^{-9}A/V for Chip C can be obtained from the linear region of V_g [10, 20 V] in the $I_{ds}-V_g$ curves shown in Figure 7c. From the analysis above, we arrive at the fact that higher carrier concentration yields lower carrier mobility, which is due to the increased scattering from the lattice defects and electron−electron interaction.

Summary

Zinc oxide, a widely utilized semiconductor material, is a metal oxide that has been doped often with *n*-type, *p*-type, and even ferromagnetic impurities.[24,25] For the purpose of fabricating nanoscale electronic devices, one emphasis is to increase nanowire channel carrier concentration and improve electrical efficiency as well. In this paper, we described a modified synthesis method and characterized the subsequent electrical properties of ZnO nanowires. Instead of implanting other elements, our zinc vapor trapping CVD process paves a way to produce relatively high *n*-type carrier concentration in nanowires during synthesis. Electron microscopy observations show the morphology change and that single-crystal nanowires can be obtained in certain locations with proper mass transfer to surface reasion ratio. Thus, by in-situ changing the synthesis environment, nanowires properties can be manipulated. In addition, we have fabricated nanowire FETs and made contrasts between two nanowires: one synthesized via a method similar to more traditional CVD and another synthesized under the zinc vapor trapped environment. The comparisons of their electrical transport properties conclude that the *n*-type behavior of the nanowires is enhanced with higher carrier concentration and better conductivity. This result contributes to the development of efficient electronic devices based on ZnO nanowires.

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